Abstract

High speed processor

High speed processor having a data processing unit (13) for processing data, a data memory (20) which is connected to the data processing unit via a data bus (10) and can be addressed by the data processing unit (13) via a data memory address bus (18), at least one input interface buffer (9) which is connected to the data bus (10) and has the purpose of buffering input data, at least one output interface buffer (16) which is connected to the data bus (10) and has the purpose of buffering output data, the input interface buffer (9) and the output interface buffer (26) being directly addressable by the data processing unit (13) via an interface address bus (24).

Figure 4

List of reference numerals

1	High speed processor
2	Digital input
3	Data line
4	Analog line
5	Analog/digital converter
6	Data source
7	Line
8	Port input
9	Input interface buffer
10	Data bus
11	Data bus terminal
12	Data bus terminal
13	Data processing unit
14	Internal registers
15	ROM memory
16	Lines
17	Data memory address bus terminal
18	Data memory address bus
19	RAM memory
20	Data memory
21	Data bus terminal
22	Data memory address bus terminal
23	Interface address bus terminal
24	Interface address bus
25	Interface address bus terminal
26	Output interface buffer
27	Interface address bus terminal
28	Data bus terminal
29	Lines
30	Digital data output
31	Lines
32	Digital/analog converter
33	Analog lines
34	Data sink